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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,046	08/28/2003	Toru Takayama	0756-7193	7230

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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
12/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/650,046	TAKAYAMA ET AL.	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,5,8,13,23,28,33,36-43,45,47-57,74-80 and 82-87* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☒ Claim(s) *3,5,8,13,18,23,28,33 and 74-80* is/are allowed.

6)☒ Claim(s) *36-43,45,47-57 and 82-87* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

The request filed on 10/6/08 for a Request for Continued Examination (RCE) under 37 CFR 1.114 is acceptable and an RCE has been established. An action on the RCE follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 82-84 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamanaka (U.S. Patent Publication No. 2007/0087492) of embodiment 1 in view of Yamanaka (U.S. Patent Publication No. 2007/0087492) of embodiment 2.

Referring to figures 1-41, Yamanaka teaches a manufacturing method for a semiconductor device, comprising:

Heating an entire surface of a substrate by radiation heating from a first heat source (see paragraph# 364, figure 7, 1(1));

Forming semiconductor layer (7a/67) on the substrate (1/61);

Forming an insulating layer (8/106) over the semiconductor layer (7a/67) includes a region to become at least a channel region of the thin film transistor (see paragraph# 399, 510, figure 2(4), 41(C));

Forming a conductive layer (15/75) over the semiconductor layer (67) with insulating layer (68) interposed between (see figure 3, 41(C);

Selectively heating the semiconductor layer (7a/67) by using a second heat source capable of radiating an electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band (see paragraph# 410, 513, 517, figures 4(10), 41(C). It is noted that UV light band is within the visible light band (400-800nm)). It is inherent that heating substrate which include every single layer on/in the substrate will be heated as well (the conductive layer, the semiconductor layers and the insulating layer…etc.);

Wherein an entire top surface of the semiconductor layer (7a/67) is covered by the conductive layer (15/75, see figure 41(C) when the semiconductor layer (7a/67) is selectively heated (see figure 41(C)).

Regarding to claim 83, the selective heating of the semiconductor layer is performed by using the second heat source capable of radiating an incoherent electromagnetic wave (see paragraph# 471).

Regarding to claim 84, substrate is a glass substrate (see paragraph# 170).

However, Yamanaka's embodiment 1 does not teach the entire top surface of the semiconductor layer is covered by the conductive layer.

Yamanaka's embodiment 2 teaches in figure 41, forming the entire top surface of the semiconductor layer (67) is covered by the conductive layer (75).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form the conductive layer over the entire top surface of the semiconductor layer in Yamanaka's embodiment 1 because the process would increase contact surface area.

Claims 36-41, 45, 47-53, 85-87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka (U.S. Patent Publication No. 2007/0087492) as applied to claims 82-84 above in view of Yamazaki et al. (U.S. Patent Publication No. 2001/0049163A1).

Referring to figures 1-41, Yamanaka teaches a manufacturing method for a semiconductor device, comprising:

Heating an entire surface of a substrate by radiation heating from a first heat source (see paragraph# 364, figure 7, 1(1);

Forming semiconductor layer (7a/67) on the substrate (1/61);

Forming an insulating layer (8/106) over the semiconductor layer (7a/67) includes a region to become at least a channel region of the thin film transistor (see paragraph# 399, 510, figure 2(4), 41(C));

Forming a conductive layer (15/75) over the semiconductor layer (67) with insulating layer (68) interposed between (see figure 3, 41(C);

Selectively heating the semiconductor layer (7a/67) by using a second heat source capable of radiating an electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band (see paragraph# 410, 513, 517, figures 4(10), 41(C). It is noted that UV light band is within the visible light band (400-800nm)). It is inherent that heating substrate which include every single layer on/in the substrate will be heated as well (the conductive layer, the semiconductor layers and the insulating layer…etc.);

Wherein an entire top surface of the semiconductor layer (7a/67) is covered by the conductive layer (15/75, see figure 41(C) when the semiconductor layer (7a/67) is selectively heated (see figure 41(C)).

Regarding to claim 83, the selective heating of the semiconductor layer is performed by using the second heat source capable of radiating an incoherent electromagnetic wave (see paragraph# 471).

Regarding to claim 38, 39, 84, substrate is a glass substrate (see paragraph# 170).

Regarding to claim 40, 41, substrate is selected from one of quartz and sapphire (see paragraph# 170).

Regarding to claim 45, the insulating layer (68) cover a top surface and a side surface of each of the semiconductor layers (67, see figure 34(4)).

Regarding to claim 47, the insulating layer includes a laminate of silicon oxide film and silicon nitride film (68, see figure 34(4), paragraph# 195).

However, the reference does not teach the conductive film can be form by using metal or metal nitride, or metal silicide and the conductive film having higher absorptance with respect to

an incoherent electromagnetic wave within a wavelength band ranging from visible light band to infrared band than the substrate.

Yamazaki teaches in paragraph# 90, a method of forming a conductive film by using metal or metal nitride, or metal silicide (meeting claims 48-83, 85-87). Since the conductive film (non-transparent film) is a metal, metal nitride, or metal silicide which has a very high conductivity therefore it has higher absorptance with respect to an incoherent electromagnetic wave within a wavelength band ranging from visible light band to infrared band than the glass or ceramic substrate. As well as the same material would provide the same result of absorptance with respect to an incoherent electromagnetic wave (meeting claims36-37).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form a conductive film by using metal or metal nitride, or metal silicide in process of Yamanaka as taught by Yamazaki because the conductive film of metal or metal nitride, or metal silicide is known in the semiconductor art to high conductivity gate electrode.

Claims 42-43, 54-55, 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka (U.S. Patent Publication No. 2007/0087492) in view of Yamazaki et al. (U.S. Patent Publication No. 2001/0049163A1) as applied to claims 36-41, 45, 47-53, 85-87 above further in view of Yamazaki et al. (U.S. Patent Publication No. 2001/0049163A1).

Yamanaka in view of Yamazaki et al. teaches a method of forming a TFT having a semiconductor layers, annealing the semiconductor layer, forming an insulating film on the

semiconductor layer, forming a conductive film on the insulating film, and heating the semiconductor film.

However, the reference does not teach heating of the first and second semiconductive layers is performed at temperature range that not lower than a distortion point of the substrate, and substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band.

Yamazaki et al. teaches heating of the first and second semiconductive layers is performed (see paragraphs# 254, 294. It is inherent that heating the conductive layer, the semiconductive layer and the insulating layer will also heated), the heat treatment is performed at a temperature not less than a distortion point of the substrate (see paragraph# 254, 294, heating at the temperature 700-1000°C which is greater than 700°C (at the distortion point), meeting claims 56-57).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form plurality of semiconductive island, heating for 30-300 second at the temperature greater than distortion point of the substrate in process of Yamanaka as taught by Yamazaki et al. because heating process is known in the semiconductor art to crystallized the layer as well as to activate the impurity added to the film.

Regarding to claims 42-43, 54-55, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength

band), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form the substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band in process of Yamanaka in order to optimize the process in formation of TFT device.

Allowable Subject Matter

Claims 3, 5, 8, 13, 18, 23, 28, 33 and 74-80 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in etching the conductive layer after the selective heating of the first and second semiconductor layers to form the gate electrodes over the semiconductor layers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by

Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau, can be reached on (571) 272-1945. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2813

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/650,046	TAKAYAMA ET AL.	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	